Claims

What is claimed is:

1. A phase selection mechanism for facilitating the sampling of data, said phase selection mechanism comprising:

an arrangement for interfacing with a transmitter clock;

an arrangement for interfacing with at least one receiver clock;

a phase sampler which ascertains the position of the transmitter clock with respect to the at least one receiver clock, whereby a suitable receiver clock for sampling data is ascertainable.

2. The phase selection mechanism according to Claim 1, wherein the at least one receiver clock includes a plurality of receiver clocks.

3. The phase selection mechanism according to Claim 1, further comprising:

a phase selector adapted to generate a phase selection signal; and

a plurality of Muxes which create clock signals;

said phase selector being adapted to control the phase of the clock signals created by said Muxes.

4. The phase selection mechanism according to Claim 3, wherein:

said phase selector is adapted to generate at least four distinct phase selection signals, whereby:

a first of said four phase selection signals corresponds to a basic phase for a clock signal created by each of said Muxes; and

each of the other of said four phase selection signals corresponds incrementally to an increase in phase of ninety degrees for a clock signal created by each of said Muxes.

5. The phase selection mechanism according to Claim 3, wherein:

a first one of said Muxes is adapted to create a first clock signal, having a basic phase of 270 degrees;

a second one of said Muxes is adapted to create a second clock signal, having a basic phase of 0 degrees; and

a third one of said Muxes is adapted to create a third clock signal, having a basic phase of 180 degrees.

6. The phase selection mechanism according to Claim 5, wherein said phase sampler comprises:

an arrangement for generating a first phase sample, based on said second clock signal;

an arrangement for generating a second phase sample, based on said third clock signal; and

an arrangement for combining the first and second phase samples to generate an output; and

an arrangement for producing a phase sample signal based on the output of said combining arrangement and on said third clock signal.

7. The phase selection mechanism according to Claim 6, wherein the phase sample signal is variable between at least three states, wherein:

a first one of said at least three states corresponds to the occurrence of transitions in the transmitter clock when the second clock signal is at a lower value;

a second one of said at least three states corresponds to the occurrence of transitions in the transmitter clock when the second clock signal is at a higher value; and

a third one of said at least three states corresponds to the occurrence of transitions in the transmitter clock in proximity to a falling edge of at least one of said second and third clock signals.

8. The phase selection mechanism according to Claim 7, wherein the third state of the phase sample signal corresponds to an unstable state of the phase sample signal.

9. The phase selection mechanism according to Claim 8, wherein said phase selector is controlled by the phase sample signal such that:

the first state of the phase sample signal corresponds to the phase selection signal remaining unchanged;

the second state of the phase sample signal corresponds to the phase selection signal being incremented such that said first, second and third clock signals move forward 90 degrees in absolute phase; and

the third state of the phase sample signal corresponds to the phase selection signal being incremented 90 degrees at a time until a stable phase selection signal is achieved.

10. A method of facilitating the sampling of data, said method comprising the steps of:

providing an arrangement for interfacing with a transmitter clock;

providing an arrangement for inerfacing with at least one receiver clock; and

ascertaining the position of the transmitter clock with respect to the at least one receiver clock, whereby a suitable receiver clock for sampling data is ascertained.

11. The method according to Claim 10, wherein the at least one receiver clock includes a plurality of receiver clocks.

12. The method according to Claim 10, further comprising the steps of:

generating a phase selection signal; and

creating clock signals;

said generating step comprising controlling the phase of the created clock signals.

13. The method according to Claim 12, wherein:

said generating step comprises generating at least four distinct phase selection signals, whereby:

a first of said four phase selection signals corresponds to a basic phase for each created clock signal; and

each of the other of said four phase selection signals corresponds incrementally to an increase in phase of ninety degrees for each created clock signal.

14. The phase selection mechanism according to Claim 12, wherein said creating step comprises:

creating a first clock signal, having a basic phase of 270 degrees;

creating a second clock signal, having a basic phase of 0 degrees; and

creating a third clock signal, having a basic phase of 180 degrees.

15. The method according to Claim 14, wherein said ascertaining step comprises:

a generating a first phase sample, based on the second clock signal;

generating a second phase sample, based on the third clock signal; and

a combining the first and second phase samples to generate an output; and

producing a phase sample signal based on the output of said combining arrangement and on the third clock signal.

16. The method according to Claim 15, wherein said step of producing a phase sample signal comprises producing a phase sample signal which is variable between at least three states, wherein:

a first one of the at least three states corresponds to the occurrence of transitions in the transmitter clock when the second clock signal is at a lower value;

a second one of the at least three states corresponds to the occurrence of transitions in the transmitter clock when the second clock signal is at a higher value; and

a third one of the at least three states corresponds to the occurrence of transitions in the transmitter clock in proximity to a falling edge of at least one of the second and third clock signals.

17. The method according to Claim 16, wherein the third state of the phase sample signal corresponds to an unstable state of the phase sample signal.

18. The method according to Claim 17, wherein said step of producing a phase sample signal comprises controlling the phase selection signal such that:

the first state of the phase sample signal corresponds to the phase selection signal remaining unchanged;

the second state of the phase sample signal corresponds to the phase selection signal being incremented such that the first, second and third clock signals move forward 90 degrees in absolute phase; and

the third state of the phase sample signal corresponds to the phase selection signal being incremented 90 degrees at at time until a stable phase selection signal is achieved.